

## EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	34	703/26.ccls. and @pd>"20060601"	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/01/08 12:49

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Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	381	(dynamic near optimization) and instruction\$1	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/01/08 13:16
L5	179	((runtime or run-time) near optimization)	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/01/08 13:23
L6	42	L5 and emulat\$4	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/01/08 13:29
L8	104	L2 and emulat\$4	US-PGPUB; USPAT; EPO; DERWENT	OR	OFF	2007/01/08 13:59

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[M Moudgill](#)

[Renaming numeric and segment registers using common general \*\*register pool\*\* - group of 3 »](#)

KY Liu, G Hammond, K Shoemaker, A Pai - US Patent 5,978,900, 1999 - Google Patents  
... [54] RENAMING NUMERIC AND SEGMENT REGISTERS USING COMMON GENERAL **REGISTER POOL** ... RENAMING  
NUMERIC AND SEGMENT REGISTERS USING COMMON GENERAL **REGISTER POOL** ...  
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[Reducing the complexity of the \*\*register\*\* file in dynamic superscalar processors - group of 11 »](#)

R Balasubramonian, S Dwarkadas, DH Albonesi - Proceedings of the 34th annual ACM/IEEE international ..., 2001 - portal.acm.org  
... ports available. We also attempt copies only if there are fewer than eight registers in the LI free **register pool**. When a mispredict ...  
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[\[BOOK\] \*\*Register\*\* renaming and dynamic speculation: an alternative approach - group of 8 »](#)

M Moudgill, K Pingali, S Vassiliadis - 1993 - IEEE Computer Society Press Los Alamitos, CA, USA  
... physical **register**. These registers are in state F 0 T. The remaining registers are in the free **register pool**, with states T 0 T. Fig. 4 ...  
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[Millicode \*\*register\*\* management and pipeline reset - group of 2 »](#)

SJ Nadas, RJ Pedersen - US Patent 5,226,164, 1993 - Google Patents  
... However, these registers are dynamically taken from and returned to a common physical **register pool** under control of a **register** management system. ...  
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[RADIATION DAMAGE IN SCIENTIFIC CHARGE-COUPLED DEVICES - group of 4 »](#)

J Janesick, T Elliott, F **Pool** - IEEE Transactions on Nuclear Science, 1989 - ieeexplore.ieee.org  
... IN SCIENTIFIC CHARGE-COUPLED DEVICES James Janesick, Tom Elliott, Fred **Pool** Jet Propulsion ... of 70 e- loss is measured at the end of the horizontal **register**. ...  
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[Reduction of the number of parameters needed for a polynomial random regression test day model](#)

MH **Pool**... - Livestock Production Science, 2000 - ingentaconnect.com  
... Authors: **Pool** MH; Meuwissen THE. ... You may be required to **register** and activate access/purchase before you can obtain the full text. Proceed. ...  
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[\[PS\] Stack Renaming of the Java Virtual Machine - group of 3 »](#)

R Kapoor, S Sastry, C Zilles - 1996 - cs.wisc.edu  
... The free **register pool** is a list of the **register** identifiers of free registers. A free **register** is one which isn't currently assigned ...  
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[Fluorescence Analysis of the Labile Iron \*\*Pool\*\* of Mammalian Cells - group of 4 »](#)

S Epsztejn, O Kakhlon, H Glickstein, W Breuer, ZI ... - Analytical Biochemistry, 1997 - ingentaconnect.com  
... The labile iron **pool** (LIP) of cells constitutes a cytosolic fraction of iron which is accessible to permeant chelators and contains ... Sign out. Need to **register**? ...  
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Computers, IEEE Transactions on  
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 Varaiya, P.;  
Proceedings of the IEEE  
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Computer  
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- ☐ **Software-directed register deallocation for simultaneous multithreaded processors**  
 Lo, J.L.; Parekh, S.S.; Eggers, S.J.; Levy, H.M.; Tullsen, D.M.;  
Parallel and Distributed Systems, IEEE Transactions on  
 Volume 10, Issue 9, Sept. 1999 Page(s):922 - 933  
 Digital Object Identifier 10.1109/71.798316  
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1096 KB) IEEE JNL  
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- ☐ **Welcome to the opportunities of binary translation**  
 Altman, E.R.; Kaeli, D.; Sheffer, Y.;  
Computer  
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[Dynamo: a transparent \*\*dynamic optimization\*\* system - group of 36 »](#)

V Bala, E Duesterwald, S Banerjia - Proceedings of the ACM SIGPLAN 2000 conference on ..., 2000 - portal.acm.org

... Dynamo is a **dynamic optimization** system (ie, the ... fast native instruction interpreter implemented in **hardware**. ... to implement the interpreter by using **emulation**. ...

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[Mojo: A \*\*dynamic optimization\*\* system - group of 9 »](#)

WK Chen, S Lerner, R Chaiken, DM Gillies - ... ACM Workshop on Feedback-Directed and **Dynamic Optimization** ..., 2000 - cse.ucsd.edu

... Abstract **Dynamic optimization** systems have the flexibility to adapt program execution to changing scenarios and differing **hardware** configurations. ...

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[\[PS\] Design and implementation of a \*\*dynamic optimization\*\* framework for Windows - group of 8 »](#)

D Bruening, E Duesterwald, S Amarasinghe - ... ACM Workshop on Feedback-Directed and **Dynamic Optimization** ..., 2001 - cag.lcs.mit.edu

... copy-paste approach over **emulation** because of ... that are most worthwhile targeting with **dynamic optimization**. ... on modern processors: the **hardware** is aggressively ...

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[Welcome to the opportunities of binary translation - group of 7 »](#)

ER Altman, D Kaeli, Y Sheffer - Computer, 2000 - ieeexplore.ieee.org

... **Dynamic optimization** Sometimes a dynamic translator forms part of ... typically requires emulating legacy **hardware** devices ... Complete OS **emulation** OS **emulation** can be ...

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[Transparent \*\*dynamic optimization\*\*: The design and implementation of Dynamo - group of 5 »](#)

V Bala, E Duesterwald, S Banerjia - Hewlett Packard Laboratories Technical Report HPL-1999-78. ..., 1999 - fog.hpl.external.hp.com

... whereas in the case of **dynamic optimization**, it is not ... during the initial run via **emulation**, and perform ... **Hardware** implementations of dynamic optimizers are now ...

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[Optimization and precise exceptions in dynamic compilation](#)

M Gschwind, E Altman - ACM SIGARCH Computer Architecture News, 2001 - portal.acm.org

... optimization or rely on **hardware** sup- port. ... formed in previous architecture **emulation** systems, such ... The DYNAMO **dynamic optimization** system per- forms **dynamic** ...

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[Adaptive compression of syntax trees and iterative dynamic code optimization: Two basic technologies ... - group of 6 »](#)

M Franz - Mobile Object Systems: Towards the Programmable Internet, 1997 - ics.uci.edu

... the system architecture incorporating **dynamic optimization** is ongoing ... load time is that **hardware** technology is ... application with VT100 **emulation**, an electronic ...

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[Dynamic binary translation and optimization - group of 10 »](#)

K Ebcioglu, E Altman, M Gschwind, S Sathaye - Computers, IEEE Transactions on, 2001 - ieeexplore.ieee.org

... compilation, binary translation, **dynamic optimization**, just-in ... operations do not incur **emulation** burden, whereas ... VLIW processor contains **hardware** support for ...

Published before January 2002

Terms used dynamic optimization emulation and hardware

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## 1 [The benefits and costs of DyC's run-time optimizations](#)



Brian Grant, Markus Mock, Matthai Philipose, Craig Chambers, Susan J. Eggers  
September 2000 **ACM Transactions on Programming Languages and Systems (TOPLAS)**, Volume 22 Issue 5

Publisher: ACM Press

Full text available:  [pdf\(1.59 MB\)](#)

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DyC selectively dynamically compiles programs during their execution, utilizing the run-time-computed values of variables and data structures to apply optimizations that are based on partial evaluation. The dynamic optimizations are preplanned at static compile time in order to reduce their run-time cost; we call this staging. DyC's staged optimizations include (1) an advanced binding-time analysis that supports polyvariant specialization (enabling both single-way and multi ...


**Keywords:** dynamic compilation, specialization

## 2 [Improving Java performance using hardware translation](#)



Ramesh Radhakrishnan, Ravi Bhargava, Lizy K. John  
June 2001 **Proceedings of the 15th international conference on Supercomputing ICS '01**

Publisher: ACM Press

Full text available:  [pdf\(254.91 KB\)](#)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

State of the art Java Virtual Machines with Just-In-Time (JIT) compilers make use of advanced compiler techniques, run-time profiling and adaptive compilation to improve performance. However, these techniques for alleviating performance bottlenecks are more effective in long running workloads, such as server applications. Short running Java programs, or client workloads, spend a large fraction of their execution time in compilation instead of useful execution when run using JIT compilers. In ...

## 3 [Optimization and precise exceptions in dynamic compilation](#)





Michael Gschwind, Erik Altman  
March 2001 **ACM SIGARCH Computer Architecture News**, Volume 29 Issue 1

Publisher: ACM Press

Full text available:  [pdf\(508.52 KB\)](#) Additional Information: [full citation](#), [abstract](#), [index terms](#)

Maintaining precise exceptions is an important aspect of achieving full compatibility with a legacy architecture. While asynchronous exceptions can be deferred to an appropriate boundary in the code, synchronous exceptions must be taken when they occur. This introduces uncertainty into liveness analysis since processor state that is otherwise dead may be exposed when an exception handler is invoked. Previous systems either had to


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T. J. Gordon  
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Frank Fallside  
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
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